Abstract of the Disclosure:

A test system for conducting a function test of a semiconductor element on a wafer and a method for conducting the test includes a voltage source providing a supply voltage of the element being tested, two supply contact pins connected to the voltage source for applying the supply voltage to terminal pads of the element being tested, a read contact pin producing a currentless electrical read connection of the test system to a terminal pad of the element being tested, and a means for regulating the output voltage delivered by the voltage source based upon the electrical potential of the read contact pin. As such, the supply voltage of the semiconductor element can be adjusted more precisely in the function test.

GLM/vs